

Abstract

An interleaved delay line for use in phase locked and delay locked loops is comprised of a first portion providing a variable amount of delay substantially independently of process, temperature and voltage (PVT) variations while a second portion, in series with the first portion, provides a variable amount of delay that substantially tracks changes in process, temperature, and voltage variations. By combining, or interleaving, the two types of delay, single and dual locked loops constructed using the present invention achieve a desired jitter performance under PVT variations, dynamically track the delay variations of one coarse tap without a large number of delay taps, and provide for quick and tight locking. Methods of operating delay lines and locked loops are also disclosed.